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Modeling of Thermal Resistance for Nano-Scaled DG MOSFET and CSDG MOSFET

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ABSTRACT

Micro and Nano technology devices exhibit excellent performance and scalability but in contrast they have heating effect. To analyze and minimize this thermal effect in terms of thermal resistance a model has been presented in this work for the application of mechatronics switch. It will be suitable for the sensors and systems. A simple and accurate method has been discussed for extraction of the effective thermal resistance of a double-gate MOSFET and cylindrical surrounding double-gate MOSFET. The drain, source and channel resistance has been extracted and gate resistance has been taken as negligible due to negligible gate current.

Keywords – Microelectronics, Nanotechnology, Sensor, Switch, Thermal resistance modeling, MOSFET junction temperature, VLSI.

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1. INTRODUCTION

Mechatronics includes various technical areas such as modelling, manufacturing, system integration actuator, sensors, micro-devices, opto-electronic system, robotics, automotive system, etc. [1]. In a mechatronics motion control some parameters such as robustness, actuation, position control, force control etc. have an effective model [2]. *Regtien* [3] provides an overview of the various sensors and systems which are required and/or applied in mechatronics. Also, the emphasis is on the understanding the physical principles and possible configurations of sensors has been discussed. The mechatronics system design methodology to integrate the different field / discipline knowledge, through the design and development process of mechatronics product has been discussed in [4, 5].

There are various applications of optical switches that require precision positioning of micro-actuators. The analog nature of micro electro mechanical switches (MEMS) and indeterminate device characteristics (due to manufacturing tolerance), make these switches impracticable and expensive calibrations process [6]. In the present research, I have tried to obtain the internal thermal resistance for the switch (using double gate MOSFET and cylindrical surrounding double gate MOSFET). So that the behavior of the switch pertaining to the thermal effect can be analyze, change or set in advance according to the application in the mechatronics system.

Semiconductor devices have definite operating temperature limits. High operating temperatures are undesirable since performance is degraded, reliability is impaired, and device destruction may be a possibility [7]. Typically, for every 10°C rise above 100°C, the operating life of the device reduces to halved. It is thus imperative that semiconductor devices run as cool as possible. The evaluation of temperature increase in circuit simulation is an important issue for several Silicon technologies. Self-heating can be particularly severe in case of advanced micro and nano-technology. For Silicon on Insulator (SOI) substrate, due to the poor thermal conductivity of the substrate, MOSFET devices are strongly affected by self-heating issues [8]. In the power transistors a relevant temperature increase can be observed due to the large operating voltages [9, 10]. The total thermal conductance of a traditional MOSFET is defined by constructing the equivalent thermal circuit which basically contains only resistors [11]. Generally, the basic techniques for power semiconductor thermal resistance measurements are optical, chemical, physical and electrical. Each of these techniques has its advantages and disadvantages [12].

Magnone et. al. [13] has proposed a methodology to define an equivalent resistive thermal network that allows modeling the lateral heat propagation through the Silicon substrate of power devices. The basic idea is to split the substrate in basic elements of length ΔL and to associate to each element, lumped thermal resistances. *Caviglia and Iliadis* [14] has derived a model for small signal dynamic self-heating for the general case of a two-port device and then specialized to the case of an SO1 MOSFET.

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Kang et. al. [15] has presented the method for extraction of gate electrode resistance as well as the channel resistance. This model extracted the analytical parameter with help of Y-parameter analysis and presented the extraction results of the high frequency gate resistance (R_G), with various geometries at different bias conditions. *Kang et. al.* also developed an analytical physics based gate resistance model. *Yan et. al.* [16] has presented a model that the overall gate resistance can be lowered through silicidation or the use of multiple gates. For example, the thickness of gate silicide must scale with channel length, thereby yielding a higher sheet resistivity for shorter devices. Also, increasing the number of gates tends to increase the source or drain junction capacitance and degrade circuit density.

Razavi et. al. [17] has described the impact of distributed gate resistance on four aspects of the performance of the devices: cut-off frequency, maximum frequency of oscillation, input referred thermal noise, and time response. In the digital applications the devices usually switch fast enough such that the self-heating can be ignored in circuit simulation. For analog applications accurate simulations require that instantaneous temperature be included in the modeling. But in both the cases, ignoring thermal effects can lead to various errors in parameter extraction [18].

In this work, double-gate (DG) MOSFET [19, 20] and cylindrical surrounding double-gate (CSDG) MOSFET [21, 22] has been taken to model the thermal resistance effect. These MOSFETs are in the range of nanotechnology and have small scaled parameters. The resulting analytical model accounts for the thermal conductance of each region of the transistor: gate, gate dielectric, source, drain, body, Si-substrate, interconnects, etc. But in the presented model substrate is negligible, so have not been considered. I obtained that the effect of heating in these MOSFETs is less compared to the traditional MOSEFTs. These MOSFETs can also be use for the RF switches and amplifiers.

The organization of this paper is as follows. The modeling of thermal resistance which has been used for the analysis of DG MOSFET and CSDG MOSFET has been discussed in the Section II. The thermal modeling of DG MOSFET has been analyzed in the Section III. The thermal modeling of CSDG MOSFET has been analyzed in the Section IV.
The effects of thermal resistance on various parameters have been discussed in the Section V. Finally, Section VI concludes the work and recommends the future works.

2. MODELING OF THERMAL RESISTANCE

When power is applied to a semiconductor device, the chip / junction temperature will rise to a value based on the power dissipated in the chip and the ability of the device package and its heat sink to remove this heat [7]. A steady state condition is reached when the heat generated is equal to the heat removed. Heat flows from a higher temperature to a lower temperature region, and the quantity that resists this flow of heat energy is called thermal resistance [13, 18]. A thermal circuit can model the transfer of heat from a semiconductor chip to its surroundings with direct analogy to an electrical circuit. In this work, this theory is used in the boundary of the MOSFETs, means the drain, source, gate, and channel region has been considered to observe the thermal resistance. The external components such as heat sink, ambient or air have not been considered. In an electrical circuit, if current I flow from a point at voltage V_H to a point at voltage V_L as shown in the fig. 1(a), then using Ohm's law the electrical resistance R between the two points is:

$$R = (V_H - V_L) / I$$

Therefore,

$$V_H = V_L + IR \qquad (1)$$

Now for the thermal circuit, equivalent to the electrical circuit, there is an analogous relation as [7]:

Power dissipated (P_D) → Current source (I),
Temperature (T) → Voltage (V), and
Thermal resistance (θ) → Electrical resistance (R).

Hence using thermal Ohm's law, if heat flows from a point at temperature T_H to a point at temperature T_L and dissipates power P_D as shown in the fig. 1(b), then the thermal resistance θ between the two points is:

$$\theta = (T_H - T_L) / P_D$$

Therefore,

$$T_H = T_L + P_D \theta \qquad (2)$$

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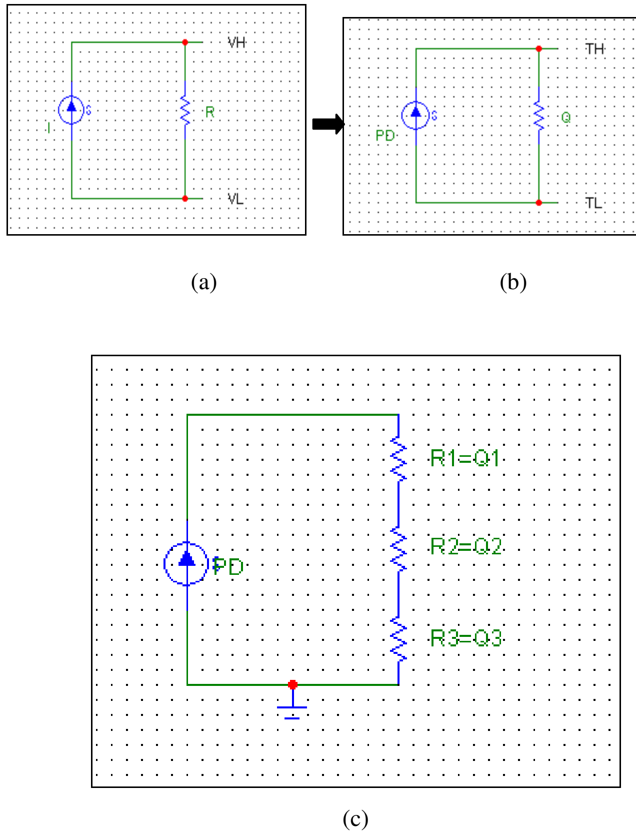


(a) (b)

(c)

Fig. 1. (a) Resistive model, (b) Thermal equivalent of the Resistive model, and (c) combination of thermal resistances.

For a typical arrangement of an integrated circuit (DG MOSFET and CSDG MOSFET) comparing the thermal resistance (for example θ_1, θ_2, and θ_3) with the electrical resistance (for example R_1, R_2, and R_3) in series combination as shown in fig. 1(c). The sum of these three thermal resistances is the total thermal resistance will be like the $R_{series} = R_1 + R_2 + R_3$, so the thermal resistance equivalent with thermal Ohm's law will be:

$$\theta_{Total} = \theta_1 + \theta_2 + \theta_3 \qquad (3)$$

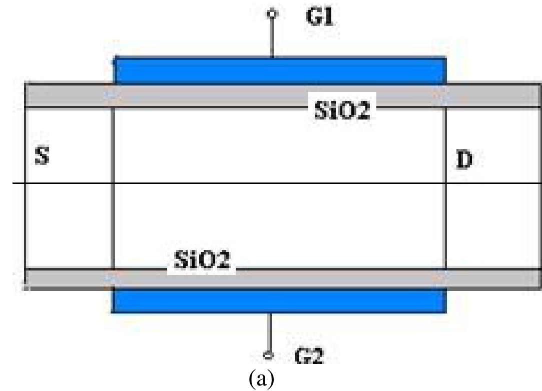
The total thermal conductance G_{th} reflects the average temperature rise ΔT in the transistor for $\Delta T = P_D / G_{th}$, where P_D is the power dissipation [11].

3. Analysis of Thermal Resistance of DG MOSFET

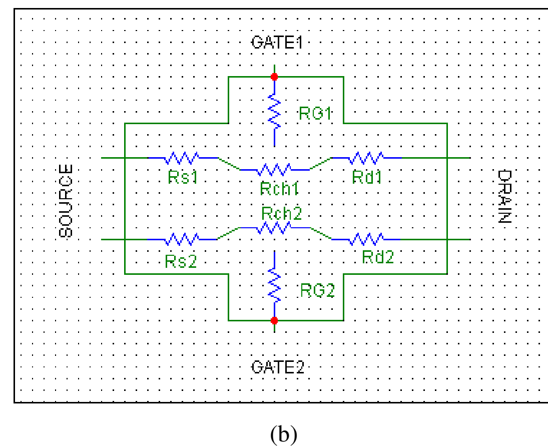
In the Double-Gate MOSFET (as shown in Fig. 2a) [19], there are two gates means one gate on each side of the Silicon oxide layers. This MOSFET creates two MOSFET back to back and the resistance structure is shown in fig. 2(b). The R_s, R_{ch} and R_d are the source resistance, channel resistance and drain resistance respectively. The R_G is the gate resistance and it has no effect in the thermal resistance model due to the negligible gate current in the MOSFET. The subscript *1* and *2* represent that the particular resistance is due to *Gate-1* and *Gate-2* respectively.

These resistances are converted to its thermal resistance as shown in the fig. 2(c) using the fig. 1 and then equated using Equation (2) and Equation (3). The gate resistance has no effect in the working of MOSFET in terms of switching. The gate creates the path from source to drain. From the fig. 2(c), using thermal Ohm's law, the final thermal resistance has been calculated as follows:

$$\theta_1 = \theta_{s_1} + \theta_{ch_1} + \theta_{d_1}$$
$$\theta_2 = \theta_{s_2} + \theta_{ch_2} + \theta_{d_2}$$



(a)



(b)

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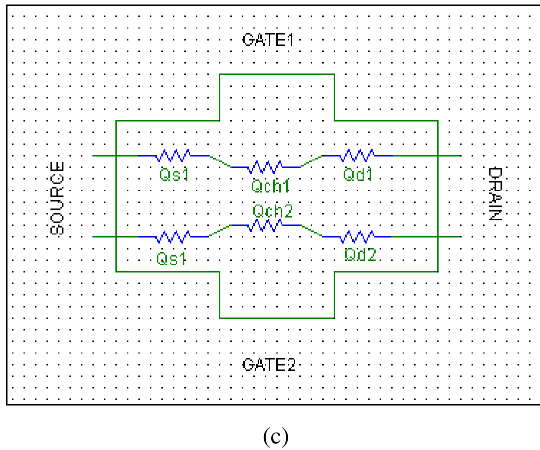


(c)

Fig. 2. Double-Gate MOSFET (a) Basic structure, (b) Resistive model, and (c) Thermal resistive model.

These θ_1 and θ_2 are in parallel, following the parallel combination of the resistances due to the *Gate-1* and *Gate-2*. So the total equivalent thermal resistance of the DG MOSFET will be:

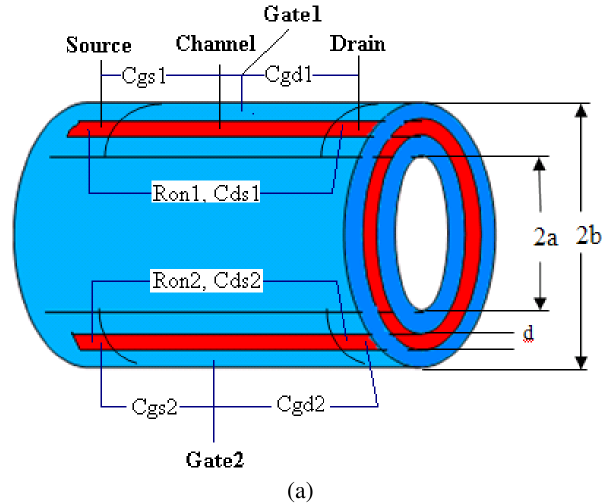
$$\theta_{DG} = \theta_1 \Pi \theta_2 = \frac{(\theta_{s_1} + \theta_{ch_1} + \theta_{d_1})(\theta_{s_2} + \theta_{ch_2} + \theta_{d_2})}{(\theta_{s_1} + \theta_{ch_1} + \theta_{d_1}) + (\theta_{s_2} + \theta_{ch_2} + \theta_{d_2})} \quad (4)$$

In this Equation (4), the thermal resistance will decreases compared to the normal MOSFET as it is parallel combination of resistance. Hence this DG MOSEFT is suitable for the application of RF switches.

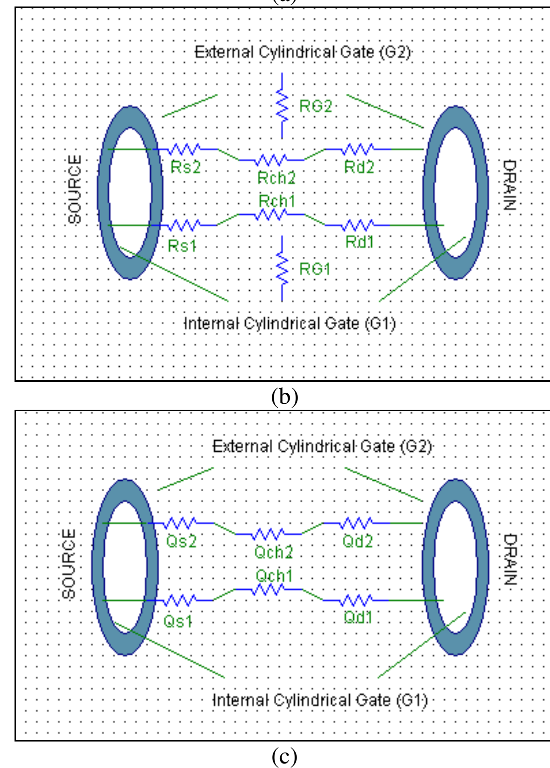
4. ANALYSIS OF THERMAL RESISTANCE OF CSDG MOSFET

In the CSDG MOSFET (as shown in Fig. 3a) [22], there are two circular gates (due to hollow cylindrical structure) i.e. one gate on the external peripheral and second one is inside the internal peripheral of the Silicon oxide layers. This MOSFET creates two MOSFET like a cylindrical structure and its resistance structure is shown in fig. 3(b). The R_s, R_{ch} and R_d are the source resistance, channel resistance and drain resistance respectively. The R_G is the gate resistance. The subscript *1* and *2* represent that the particular resistance is due to *Gate-1* and *Gate-2* respectively. The difference in the values of these resistances with compare to DG MOSFET parameter is that, these are circular resistance for the CSDG MOSGFET as in Equation (5). These resistances are converted to its thermal resistance as shown in fig. 3(c) using the fig. 1 and then equated using Equation (2) and Equation (3).

$$R = \frac{\rho L}{A} \quad (5)$$



(a)



(c)

Fig. 3. Cylindrical Surrounding Double-Gate MOSFET (a) Basic structure, (b) Resistive model, and (c) Thermal resistive model.

where ρ is the resistivity of the material, L is the channel length and A is the circular perimeter of the CSDG MOSFET as in this fig. 3(a), it will be $2\pi a$ (internal perimeter for internal resistance) and $2\pi b$ (external perimeter for external resistance). Similar to DG MOSFET, the gate resistance has no effect in the working of CSDG MOSFET in terms of switching. The gate creates the path from source to drain. From the fig. 3(c), using Thermal's ohm law, the final thermal resistance has been calculated as follows:

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$$\theta_{inrnal} = \theta_{s_1} + \theta_{ch_1} + \theta_{d_1}$$
$$\theta_{external} = \theta_{s_2} + \theta_{ch_2} + \theta_{d_2}$$

These θ_1 and θ_2 are in parallel, as external and internal cylinder structures are parallel to each other. Following the parallel combination of the resistances due to the *Gate-1* and *Gate-2*, thermal resistances will be parallel. So, the total equivalent thermal resistance of the CSDG MOSFET will be:

$$\theta_{CSDG} = \theta_{inernal} \Pi \theta_{external}$$
$$= \frac{(\theta_{s_1} + \theta_{ch_1} + \theta_{d_1})(\theta_{s_2} + \theta_{ch_2} + \theta_{d_2})}{(\theta_{s_1} + \theta_{ch_1} + \theta_{d_1}) + (\theta_{s_2} + \theta_{ch_2} + \theta_{d_2})} \quad (6)$$

In this Equation (6), the thermal resistance will decreases compared to the normal MOSFET and DG MOSFET as it is parallel combination of resistance also a cylindrical area. Hence this CSDG MOSEFT is suitable for the application of RF switches as compared to the DG MOSFET.

5. EFFECT OF THERMAL RESISTANCES

The thermal resistance affects the switching speed of the RF switch. A higher switching speed can be achieved due to the increased mobility and decreased thermal or electrical resistance. As in the thermal equivalent circuits of DG MOSFET and CSDG MOSFET, the thermal resistances are in parallel combinations, which reduce thermal resistance and hence the heating effect on the application of the devices. So, the RF switches designed by using DG MOSFET and / or CSDG MOSFET are having higher switching speed compared to the traditional MOSFET. The low thermal effect has improved performance, increased reliability, and higher density of MOSFET integrated circuits. Reliability can be increased if thermally activated processes slowdown. This can be done better with the help of CSDG MOSFET as compared to the DG MOSFET. The noise behavior can be improved as these structures has reduced thermal noise due to reduction in the equivalent thermal resistance as shown in the fig. 2(c) and fig. 3(c), with the help of Equation (4) and Equation (6). Due to the improved heating effect, one can achieve the higher packing density.

6. CONCLUSIONS & FUTURE RECOMMENDATIONS

In this work, I have modeled the thermal resistance for the DG MOSFET and CSDG MOSFET using thermal Ohm's law. Using this technology, the thermal effect on the RF switch can be analyzed in detail in future work. The proposed model can be further analyzed by physics based gate resistance model which can accurately predict the bias dependency, dependence on the number of fingers, channel lengths, and widths, junction temperatures, thermal stabilities, and thermal runaway effects of self-heating [23]. This DG MOSFET and CSDG MOSFET thermal resistance management process can further be used for RF amplifier development with junction to case temperature [24].

7. FUTURE WORK

In future work, this work can be extended to some of the application from Automation and robotics, Automotive engineering Computer aided & integrated manufacturing systems, reliability, control systems techniques, Games technologies, Systems Industrial engineering, Machine vision, Sensing and control systems etc. [25].

REFERENCES

[1] F. Harashima, "Recent advances of mechatronics," *Proc. of IEEE Int. Symp. on Industrial Electronics,* 17-20 Jun 1996, pp. 1-4.

[2] K. Ohnishi, M. Shibata, and T. Murakami, "Motion control for advanced mechatronics," *IEEE Trans. on Mechatronics*, vol. 1, no. 1, pp. 56-67, March 1996.

[3] Paul Regtien, *Sensors for Mechatronics*, 1st Ed., Jan. 2012, Elsevier.

[4] Farhan A. Salem and Ahmad A. Mahfouz, "Mechatronics design and implementation education-oriented methodology: A proposed approach," *Journal of Multidisciplinary Engineering Science and Technology,* vol. 1, no. 3, pp. 34-45, Oct. 2014.

[5] Yu Wang, Ying Yu, Chun Xie, Xiaoyang Zhang, and Weizhi Jiang, "A proposed approach to mechatronics design education: Integrating design methodology, simulation with projects," *Mechatronics*, vol. 23, no. 8, pp. 942-948, Dec. 2013.

[6] Mehrdad Saif, Behrouz Ebrahimi, and Mehdi Vali, "A second order sliding mode strategy for fault detection and fault-tolerant-control of a MEMS optical switch," *Mechatronics*, vol. 22, no. 6, pp. 696-705, Sept. 2012.

[7] Sedra and Smith, *Microelectronic Circuits*, 6th Ed., 2011, Oxford University Press, New York, USA.

[8] M. Braccioli, G. Curatola, Y. Yang., E. Sangiorgi, C. Fiegna, "Simulation of self-heating effects in different SOI MOS architectures," *Solid State Electronics*, vol. 53, no. 4, pp. 445-451, April 2007.

[9] R. Gaska, A. Osinsky, J. W. Yang, M. S. Shur, "Self-heating in high-power AlGaN-GaN HFET's," *IEEE Electron Device Letter*, vol. 19, no. 3, pp. 89-91, March 1998.

[10] C. C. Cheng, J. F. Lin, T. Wang, T. H. Hsieh, J. T. Tzeng, Y. C. Jong, R. S. Liou, S. C. Pan, and S. L. Hsu, "Impact of self-heating effect on hot carrier degradation in high-voltage LDMOS," *IEEE Technical Digest of Electron Devices Meeting (IEDM) Tech. Dig.,* 10-12 Dec. 2007, pp. 881-884.

[11] N. Bresson, S. Cristoloveanu, C. Mazure, F. Letertre, and H. Iwai, "Integration of buried insulators with high thermal conductivity in SOI MOSFETs: Thermal properties and short channel effects," *Solid State Electronics*, vol. 49, no. 9, pp. 1522–1528, Sept. 2005.

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[12] Z. Jakopovic, "Computer controlled measurement of power MOSFET transient thermal response," *23rd Annual IEEE Power Electronics Specialists Conference (PESC),* 29 June-3 July 1992.

[13] Paolo Magnone, Claudio Fiegna, Giuseppe Greco, Gaetano Bazzano, Enrico Sangiorgi, Salvatore Rinaudo, "Modeling of thermal network in silicon power MOSFETs," *12th International Conference on Ultimate Integration on Silicon (ULIS),* Cork, Ireland, 14-16 March 2011, pp. 1-4.

[14] Anthony L. Caviglia and Agis A. Iliadis, "Linear dynamic self-heating in SOI MOSFET's," *IEEE Electron Device Letters*, vol. 14, no. 3, pp. 133-135, March 1993.

[15] Myounggon Kang, In Man Kang, and Hyungcheol Shin, "Extraction and modeling of physics-based gate resistance components in RF MOSFETs," *Proc. of Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF),* San Diego, California, USA, 18-20 Jan 2006, pp. 218-221.

[16] Ran H. Yan, Kwing F. Lee, Duk Y. Jeon, Y. O. Kim, B. G. Park, M. R. Pinto, Conor S. Rafferty, D. M. Tennant, E. H. Westerwick, G. M. Chin, M. D. Morris, K. Early, P. Mulgrew, W. M. Mansfield, R. K. Watts, Alexander M. Voshchenkov, Jeffrey Bokor, Robert G. Swartz, and A. Ourmazd "89-GHz f_T room-temperature silicon MOSFETs," *IEEE Electron. Device Letter,* vol. 13, no. 5, pp. 256-258, May 1992.

[17] Behzad Razavi, Ran Hong Yan, and Kwing F. Lee, "Impact of distributed gate resistance on the performance of MOS Devices," *IEEE Transactions on Circuits and Systems-I Fundamental Theory and Applications*, vol. 41, no. 11, pp. 750-754, Nov. 1994.

[18] T. Y. Lee and R. M. Fox, "Extraction of thermal resistance for fully-depleted SOI MOSFETS," *Proc. of IEEE International SOI Conference*, Tucson, Arizona, 3-5 Oct. 1995, pp. 78-79.

[19] Viranjay M. Srivastava, K. S. Yadav, and G. Singh, "Design and performance analysis of double-gate MOSFET over single-gate MOSFET for RF switch," *Microelectronics Journal*, vol. 42, no. 3, pp. 527-534, March 2011.

[20] F. Djeffal, Z. Ghoggali, Z. Dibi, and N. Lakhdar, "Analytical analysis of nanoscale multiple gate MOSFETs including effects of hot carrier induced interface charges," *Microelectronics Reliability*, vol. 49, no. 4, pp. 377-381, April 2009.

[21] A. Nitayami, H. Takato, N. Okabe, K. Sunouchi, K. Hiea, and F. Horiguchi, "Multipillar surrounding gate transistor (M-SGT) for compact and high-speed circuits," *IEEE Trans. on Electron Devices*, vol. 38, pp. 579-583, 1991.

[22] Viranjay M. Srivastava, "Signal processing for wireless communication MIMO system with nano-scaled CSDG MOSFET based DP4T RF Switch," *Recent Patents on Nanotechnology*, vol. 9, no. 1, pp. 26-32, March 2015.

[23] Kuang Sheng, "Maximum junction temperatures of SiC power devices," *IEEE Transactions on Electron Devices*, vol. 56, no. 2, pp. 337-342, Feb. 2009.

[24] Zhongwei Qi, Huaiyu Dong, Yahong Wang, and John W. Reif, "Thermal management of MOSFET junction temperature in RF amplifier," *Proc. of 27th IEEE Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM)*, CA, USA, 20-24 March 2011, pp. 166-174.

[25] David Bradley, David Russell, Ian Ferguson, John Isaacs, Allan MacLeod, and Roger White, "The internet of things – The future or the end of mechatronics," *Mechatronics*, vol. 27, pp. 57-74, April 2015.

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